Remarks

The present amendment responds to the Official Action dated May 15, 2006. A petition for a one month extension of time to respond and authorization to charge Deposit Account No. 50-1058 the large entity extension fee of $120 accompany this amendment. The Official Action objected to the Title. A restriction requirement was raised by phone and Group I claims were elected. This election is affirmed by this amendment. Due to the election of the Group I claims, claims 23-27 were withdrawn from further consideration by the Examiner and are now canceled without prejudice. The Official Action objected to claims 3 and 17 as informal. Claims 13 and 14 were rejected under 35 U.S.C. § 101. Claims 1-5 and 9-12 were rejected under 35 U.S.C. § 102(b) based on Lowell et al. U.S. Patent No. 3,623,017 (Lowell). Claim 15 was rejected under 35 U.S.C. § 102(b) based on Ishikawa U.S. Patent No. 5,787,303 (Ishikawa). Claims 6-8, 13, and 14 were rejected under 35 U.S.C. § 103(a) based on Lowell. Claims 15-22 were rejected under 35 U.S.C. § 103(a) based on Lowell in view of Ishikawa. These grounds of rejection are addressed below.

Claims 23-27 have been canceled without prejudice and claims 1, 3-7, 9, 12-15, and 17-22 have been amended to be more clear and distinct. In particular, it is noted that in claim 1, for example, "a shorter execution latency" and "a second execution latency" have been changed to "a first execution latency" and "a second execution latency" "wherein the first execution latency is shorter than the second execution latency" simply to improve the clarity of expression throughout the claims when these two execution latencies are referred to throughout claims 1-12. Such

changes are not intended to limit the scope of the claims in any way. Claims 1-22 are presently pending.

Amendments to the Specification

The title has been amended as follows:

METHODS AND APPARATUS FOR ADAPTING PIPELINE STAGE LATENCY BASED ON INSTRUCTION TYPE

Claim Objections

Claims 3 and 17 have been amended, changing "... communications and variations and combinations thereof" to "... communications or combinations thereof" as suggested by the Examiner.

Claim Rejections

Claim 13 and 14 were rejected under 35 U.S.C. § 101. Claim 13 has been amended to add a step of "executing the application program on a processor" as suggested by the Examiner.

The Art Rejections

As addressed in greater detail below, Lowell and Ishikawa do not support the Official Action's reading of them and the rejections based thereupon should be reconsidered and withdrawn. Further, the Applicants do not acquiesce in the analysis of Lowell and Ishikawa

made by the Official Action and respectfully traverse the Official Action's analysis underlying its rejections.

Claims 1-5 and 9-12 were rejected under 35 U.S.C. § 102(b) based on Lowell. Lowell describes a processor that upon detection of an "extended sequence instruction" causes a hold to be generated and a higher speed clock switched in to replace a low speed clock used for normal timing of the processor. Lowell executes at the lower speed clock for "normal" instructions and executes the "extended sequence instructions" with the high speed clock. Lowell, Abstract. Lowell defines "extended sequence instructions" as being "multiply, divide, square root, etc." which are typically longer execution type instructions as compared to AND, OR, NOT, simple adds, and the like. The longer execution type of instructions typically require multiple execution stages or multiple cycles of execution before generating a result which, according to Lowell, "During the execution of this type of instruction by the arithmetic section of the computer, it is necessary to interrupt the normal timing of the computer until the extended sequence instruction has been completed." Lowell suggests that by switching to a high speed clock for "extended sequence instructions", the interruption of normal timing may be minimized. Lowell further describes circuitry to switch to a high speed clock "so that the command enable signals for the arithmetic section are produced at a faster rate". To produce signals at a "faster rate" requires the use of multiple clock pulses further supporting Lowell's approach to execute an extended sequence instruction. Lowell, col. 1, lines 5-12 and lines 47-55. Lowell is silent on the type of pipelining used and operation of the "extended sequence instructions". Lowell is also silent with regard to the latency of pipeline stages of the processor using his invention. This lack of

information on latency of pipeline stages demonstrates that Lowell is not concerned with changing the latency of pipeline stages.

In contrast to Lowell, the present invention describes a processor pipeline which adapts the latency of stages of the processor pipeline dependent on a classification of an instruction fetched for execution. As recited in the amended claim 1, the classification is done in "a decode stage for classifying and decoding the instruction" and "generating an instruction class indication", where the decode stage is a stage of the processor pipeline. Also in claim 1, "an adaptable pipeline control unit" is "responsive to the instruction class indication for adapting the latency of a pipeline stage dependent on the instruction class".

Lowell does not teach and does not make obvious classifying an instruction based on an instruction's execution latency to generate an instruction class indication. Lowell also does not teach and does not make obvious "adapting the latency of a pipeline stage dependent on the instruction class" as presently claimed in claim 1.

The Official Action rejected claim 15 under 35 U.S.C. § 102(b) based on Ishikawa. Ishikawa describes a VLIW architecture for adjusting individual instruction execution dependent upon operand dependency interlocks. Ishikawa describes a four issue VLIW which may contain instructions having different execution times. Ishikawa checks for operand usage between instructions in the VLIW and based on operand dependencies allows an instruction to proceed with execution or be held up from executing until an operand dependency is resolved. Ishikawa, col. 3, lines 20-36. Ishikawa does not teach and does not make obvious a VLIW processor having "executable function instructions located in multiple instruction slot format VLIWs, the

class one instructions having a first execution latency and the class two instructions having a longer second execution latency". Ishikawa does not teach and does not make obvious "a decode stage for" "generating an instruction class indication for each of the plurality of executable function instructions". Ishikawa also does not teach and does not make obvious "an adaptable pipeline control unit" for "adapting the latency of each stage of the plurality of instruction class controllable pipelines dependent on the instruction class indications", as claimed in claim 15.

The Official Action rejected claims 6-8, 13, and 14 under 35 U.S.C. § 103(a) based on Lowell. Since dependent claims 2-5, 6-8, and 9-12 depend from and contain all the limitations of the amended claim 1, claims 2-5, 6-8, and 9-12 distinguish from the references in the same manner as claim 1 and are in order for allowance.

Further claim 13 recites, "an instruction class adaptable pipeline processor supporting at least two classes of instructions with a first class operable with a first latency for each pipeline stage of the adaptable pipeline and a second class operable with a second latency for each pipeline stage and where, the first latency is shorter than the second latency". Lowell does not teach and does not make obvious "a first plurality of instructions used in the program operable with the first latency specified in a format of each of the first plurality of instructions as class 1 instructions and with a second plurality of instructions used in the program operable with the second latency specified in a format of each of the second plurality of instructions as class 2 instructions". Lowell also does not teach and does not make obvious "modifying the application program by changing, where appropriate, the format of class 1 instructions to class 2 instructions

to minimize power use while still meeting performance requirements of the application program" as presently claimed in claim 13.

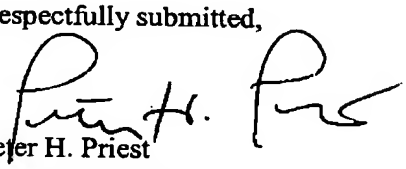
Claims 15-22 were rejected under 35 U.S.C. § 103(a) based on Lowell in view of Ishikawa. As addressed in detail above, Lowell does not teach and does not make obvious classifying an instruction based on the instruction's execution latency. Lowell also does not teach and does not make obvious adapting the latency of a pipeline stage dependent on the instruction class indication. As addressed in detail above, Ishikawa does not teach and does not make obvious "generating an instruction class indication for each of the plurality of executable function instructions". Ishikawa also does not teach and does not make obvious "adapting the latency of each stage of the plurality of instruction class controllable pipelines dependent on the instruction class indications" Consequently, Ishikawa does not cure the deficiencies of Lowell.

Since dependent claim 14 and claims 16-22 depend from and contain all the limitations of the amended claims 13 and 15, respectively, claims 14 and 16-22 distinguish from the references in the same manner as claims 13 and 15 and claims 13, 14, and 15-22 are in order for allowance.

Conclusion

All of the presently pending claims, as amended, appearing to define over the applied references, withdrawal of the present rejection and prompt allowance are requested.

Respectfully submitted,



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